Analysis of Narrow Width Effects in Polycrystalline Silicon Thin Film Transistors

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(Received April 26, 2002; accepted for publication October 2, 2002)

In this study, narrow width effects of polycrystalline silicon thin film transistors (poly-Si TFTs) are investigated. With reducing channel width, TFT characteristics such as mobility, threshold voltage, and subthreshold swing are found to improve dramatically. To gain insight on the origin of the narrow width effects, a physically-based model is proposed to simulate the output characteristics of poly-Si TFTs. Excellent fitting with the experimental data is observed over a wide range of drain bias, gate bias, and channel width. Our model shows that both the deep state density and tail state density are reduced with reducing channel width, thus accounting for the improved TFT characteristics. In addition, subthreshold swings of poly-Si TFTs with various channel widths and lengths are compared. It is found that the subthreshold swings of poly-Si TFTs with the same channel area are identical, indicating that the grain-boundary trap density is reduced due to the reduction of channel area. [DOI: 10.1143/JJAP.42.28]

KEYWORDS: narrow width, deep state, tail state, modeling, poly-Si thin-film transistors

1. Introduction

Recently, the polycrystalline silicon thin film transistor (poly-Si TFT) is widely studied due to its compatibility with the conventional silicon technology. The primary advantage of poly-Si TFTs over conventional a-Si:H TFTs lies in their higher field-effect mobility, namely higher drive current, as well as the ability to fabricate both n-channel and p-channel TFTs. It is well known that the characteristics of poly-Si TFTs are dominated by the potential barrier and trap at the grain boundary in poly-Si film. Since the number of grain boundaries in the active channel of the TFTs is reduced with reducing channel dimension, the TFT characteristics are expected to improve with shrinking channel dimension.1–4) It is also reported that poly-Si TFTs with a multichannel structure can be operated under high voltage (>100 V). This enables poly-Si TFTs to be used in peripheral high-voltage circuits. The narrow stripes in a multichannel structure enhance device performance due to the reduction of grain boundary states.5) However, there exist some conflicting observations among previous studies. For example, Yamuchii et al. studied the channel width dependence on threshold voltage, subthreshold swing, and grain-boundary trap density.6) They concluded that the reduced threshold voltage with decreasing channel width is correlated with the grain-boundary trap reduction. Since it is believed that both the threshold voltage and the subthreshold swing are related to deep states,6) a reduction in threshold voltage should be accompanied by a decrease in subthreshold swing. However, their experimental results showed that the subthreshold swing remains essentially unchanged regardless of the trap density reduction.2) While in ref. 1, the reduction in both the subthreshold swing and the threshold voltage with reducing channel dimension is shown to be due to the reduced trap density. Nevertheless, this still does not explain why the mobility of TFTs with small-grain poly-Si channel remains unchanged. In addition, in refs. 1–3, the effective grain-boundary trap density was calculated using the model developed by Levinson et al.,7) in which only the midgap deep states are considered, although it is well known that both the deep states and tail states influence the TFT’s characteristics. Besides, the Levinson’s model is valid only when the gate voltage is large and the voltage drop across the grain boundary is very small (i.e., typically smaller than $kT/q$). Therefore, a comprehensive study and the construction of a model including both deep states and tail states would be helpful in shedding light on the effects of narrow width on the TFT characteristics.

In this study, we have carefully fabricated and characterized n-channel poly-Si TFTs with various channel widths to investigate the channel width effects. Typical parameters such as mobility, subthreshold swing, and turn-on voltage are extracted from the transfer characteristics. More importantly, we have also proposed a simple physically-based analytical model by taking into consideration both the deep state and tail state. The amounts of deep state and tail state can be determined precisely by fitting the simulated output characteristics with the experimental results. The simulated transistor characteristics were compared with the experimental data over a wide range of gate bias, drain bias, and channel width. Excellent fitting between the simulated results and the experimental data support the validity of this model.

2. Experimental Procedures

Self-aligned top-gated poly-Si TFTs with lightly-doped drain structure were employed in this study. The channel length is kept at 20 μm, while the channel width is varied from 10 μm to 0.9 μm. Briefly, a 100 nm undoped poly-Si layer was first deposited by low pressure chemical vapor deposition without solid phase crystallization on oxidized silicon and patterned into individual active device islands. Then, a 50 nm TEOS oxide was deposited to serve as the gate insulator. A second poly-Si film was subsequently deposited and patterned to form the gate. Next, lightly-doped source/drain regions were formed by phosphorous (with $1 \times 10^{13}$ cm$^{-2}$ at 55 keV) implants. A 400 nm self-aligned sidewall spacer was formed by the deposition of an oxide layer and subsequent reactive-ion-etching. Subsequently, self-aligned n+ source/drain regions were formed by heavy-dose phosphorous (with $5 \times 10^{15}$ cm$^{-2}$ at 70 keV) implants. Dopant activation was then performed by rapid thermal annealing (RTA) at 750°C for 20 s. An Al film was then deposited and patterned to form the electrodes, followed by nitrogen annealing. No plasma treatment was performed to improve the characteristics of poly-Si TFT.
3. Results and Discussions

Figure 1(a) shows the normalized $I_D$–$V_D$ characteristics for poly-Si TFTs with channel width of 10 μm (white circle) and 0.9 μm (dark circle). The curves for these two devices are quite similar except that the normalized ON current of the narrow (i.e., $W = 0.9 \mu m$) device is much larger. Figure 1(b) shows the normalized $I_D$–$V_G$ characteristics. Clearly, the narrow (i.e., $W = 0.9 \mu m$) device exhibits a sharper subthreshold swing and a smaller threshold voltage than those of the wide (i.e., $W = 10 \mu m$) device. However, the leakage currents of these two devices are quite similar. It should be noted here that we were unable to measure the minimum current of the narrow (i.e., $W = 0.9 \mu m$) device, because of its small channel width and thus very low minimum current which is beyond the measurement limit of HP 4145. The normalized drain current (i.e., $I_D/C_d = W$) measured at a gate voltage $V_G = 10 \text{V}$ and a drain voltage $V_D = 5 \text{V}$ as a function of channel width is shown in Fig. 2. It is found that the $I_D/C_d = W$ value increases with decreasing channel width. Furthermore, a drastic increase in $I_D/C_d = W$ value is observed when the channel width is decreased to below 2 μm. We have also measured the leakage current as a function of channel width. However, no obvious trend is observed (data not shown). This may be due to the fact that the conduction mechanism responsible for the leakage current is thermionic-field emission near the drain. In contrast to ON current that depends on the average quality of poly-Si film within the channel, the leakage current is thus only affected by the quality of the poly-Si film in the drain depletion region. As a result, device-to-device variation, rather than channel width dependence, dominates and no width dependence is observed.

Since the drain current is related to both ON voltage and mobility, it is important to distinguish the contributions due to ON voltage and mobility in order to identify the origin of the increased drain current with reducing channel width. The ON voltage and the mobility as a function of channel width are shown in Fig. 3. The ON voltage was defined as the gate bias for a drive current of $(W/L) \times 10^{-8} \text{A}$ at $V_D = 0.1 \text{V}$. It can be seen that the ON voltage decreases with decreasing channel width, especially when the channel width is below 2 μm. The mobility was determined from the transconductance at $V_D = 0.1 \text{V}$ using the bulk-silicon transistor model. In contrast to previous studies in which the mobility remains almost constant regardless of the channel dimension, our results clearly show that the mobility is increased with reducing channel width. Consequently, both the reduction of ON voltage and increment of mobility contribute to the increase of ON current with channel width.

The subthreshold swing, which reflects the quality of the poly-Si channel film and poly-Si/oxide interface, is plotted in Fig. 4 as a function of channel width. The subthreshold
swing reduces with decreasing channel width, and starts to decrease rapidly at \( W = 2 \, \mu m \). These results, along with above-mentioned improvement of threshold voltage and mobility, strongly suggest that effective trap density in the poly-Si film is reduced with reducing channel width.

It has been reported that some defects along the channel edge caused by poly-Si channel etching\textsuperscript{2,3} may degrade the TFT characteristics. When the channel width is reduced, the effect of the poly-Si pattern edge is expected to dominate. Consequently, with fixed channel length, the defect density is increased with decreasing channel width.\textsuperscript{3} In order to pinpoint the origin of the reduced trap density with reducing channel width, the subthreshold swing as a function of channel length, with channel width kept at 20 \( \mu m \), is also shown in Fig. 4 for comparison. Note that when the channel width of the \( L = 20 \, \mu m \) devices is equal to the channel length of the \( W = 20 \, \mu m \) devices, their subthreshold swings are almost identical. Since the active channel area and shape for these two types of devices are similar, it is reasonable to assume that the reduction of grain boundary trap density is due to reduced channel area and shape, rather than due to the channel width alone.

4. Theory

Previous experimental results had demonstrated that the density of defect states in poly-Si film is continuous across the forbidden band gap,\textsuperscript{10,11} with a broad peak near the midgap and an exponential tail.\textsuperscript{12} For simplicity and to have a clear physical insight, in our model we adopt a simple mono-energy trap model. A midgap deep state located at deep state energy level \( E_{\text{sd}} \) and a tail state located at tail state energy level \( E_{\text{st}} \) with respect to intrinsic Fermi level are considered. For simplifying the derivation of the current flowing across a grain boundary, the following assumptions are made: (1) the crystallites are partially depleted; (2) the depletion approximation is valid; (3) the voltage drop across the neutral regions is negligible. According to the model in ref. 13, for a given gate voltage \( V_G \) and drain voltage \( V_D \), the average electron density \( n \) is defined as

\[
    n = C_{\text{ox}}(V_G - V_{\text{fb}})/qt_{\text{ch}} \tag{1}
\]

where \( C_{\text{ox}} \) is the gate oxide capacitance per unit area, \( V_{\text{fb}} \) is the flatband voltage, and \( t_{\text{ch}} \) is the channel thickness. By taking the effect of drain bias on the surface potential along the channel into consideration, the average electron density becomes

\[
    n = C_{\text{ox}}(V_G - V_{\text{fb}} - \alpha V_D)/qt_{\text{ch}} \tag{2}
\]

where \( \alpha \) is an extracted parameter determined from fitting the experimental output characteristics. The average Fermi level \( E_F \) with respect to intrinsic Fermi level at the center of the grains is

\[
    E_F = kT \ln(n/n_i) \tag{3}
\]

where \( n_i \) is the intrinsic carrier concentration of silicon. Based on the model proposed in ref. 14, we can calculate the grain-boundary depletion width \( W_d \) and the grain-boundary barrier potential \( \phi_b \) from the trapped carrier density on grain boundaries using the Fermi–Dirac statistics and grain-boundary depletion approximation. From the charge-neutrality condition, the depletion width near the grain boundary can be calculated as

\[
    2nW_d = \frac{N_u}{1 + \frac{1}{2} \exp\left(\frac{E_u - E_F + q\phi_b}{kT}\right)} + \frac{N_d}{1 + \frac{1}{2} \exp\left(\frac{E_d - E_F + q\phi_b}{kT}\right)} \tag{4}
\]

where \( N_u \) and \( N_d \) are the grain-boundary tail-state density and deep-state density, respectively, and \( \phi_b \) is the barrier potential. When the grain is partially depleted, the barrier potential of grain boundaries can be expressed as

\[
    \phi_b = \frac{qW_d^2}{2\varepsilon_s} \tag{5}
\]

In the polysilicon channel, the channel mobility \( \mu \) is dominated by the grain-boundary mobility rather than by the grain mobility. It is empirically described as\textsuperscript{8,15}

\[
    \mu = \mu_0 \exp\left(-\frac{q\phi_b}{kT}\right) \tag{6}
\]

Using the gradual channel approximation, the current–voltage relationship of the poly-Si TFT with a channel length \( L \) and a width \( W \) in the linear region can be expressed as

\[
    I_D = \frac{W}{L} \int_0^{V_D} C_{\text{ox}}(V_G - V_{\text{fb}} - V(x))\mu_0 \exp\left(-\frac{q\phi_b}{kT}\right) dV(x) \tag{7}
\]

where \( V_{\text{fb}} \) is the threshold voltage and \( V(x) \) is the channel potential. By assuming that the channel potential \( V(x) \) is linearly dependent on drain bias,\textsuperscript{16} and the lateral channel electric field \( E_x = V_D/L \), eq. (7) can be derived as

\[
    I_D = \frac{W}{L} \int_0^{V_D} C_{\text{ox}}(V_G - V_{\text{fb}} - V_D)\frac{x}{L} \mu_0 \exp\left(-\frac{q\phi_b}{kT}\right) \frac{V_D}{L} dx \tag{8}
\]

In the saturation region, the channel length modulation is included for calculation and the drain current is described as

\[
    I_D = I_{D\text{sat}} \left[ 1 + \frac{I_{D\text{sat}}}{V_A} (V_D - V_{D\text{sat}}) \right] \tag{9}
\]
where $I_{Dsat}$ is the saturation current, $V_{Dsat}$ is the saturation voltage, and $V_A$ is the early voltage.

Figure 5 shows the simulated normalized output characteristics for n-channel TFTs with different $\alpha$ values. The drive current for the device with $\alpha = 0$ is larger than that of the device with $\alpha = 0.27$, especially at high drain biases. Clearly, if the surface potential reduction along the channel and thus the average carrier density reduction due to drain bias are not taken into account ($\alpha = 0$), the grain-boundary barrier potential is underestimated and so the drive current is overestimated. In Fig. 6(a), the simulated normalized output characteristics by considering only the mono-energetic deep state are compared with the experimental data. Although, the simulated drain current at low gate bias (e.g., $V_G = 6\, \text{V}$ and $9\, \text{V}$) agrees very well with the experimental measurements. Without considering the tail state, however, the simulated drain current at high gate bias (e.g., $V_G = 12\, \text{V}$ and $15\, \text{V}$). On the other hand, the simulated drain current by considering only the tail state can fit the drain current accurately at high gate bias ($V_G = 15\, \text{V}$), as shown in Fig. 6(b). However, the simulated drain current at low gate bias is overestimated due to the lack of deep states. So in contrast to previous studies that considered only either deep state or tail state,\textsuperscript{6,14,16} we have successfully demonstrated that by considering both the deep state and tail state simultaneously, the drain current can be simulated accurately over a wide range of gate bias.

Figures 7(a) and 7(b) compare the calculated and experimental drain currents for TFTs with $W/L = 10\, \mu\text{m}/20\, \mu\text{m}$ and $0.9\, \mu\text{m}/20\, \mu\text{m}$, respectively, using the fitting parameters as summarized in Table I. Excellent fittings between experimental data and simulation are obtained for these two devices, indicating that this model is valid over a wide range of channel widths. The grain-boundary deep state density and tail state density as a function of channel width are plotted in Fig. 8. The fitting parameters for TFTs with different widths are kept constant except for the deep state density, tail state density, and threshold voltage. Clearly, the deep state density as well as the tail state density decreases with decreasing channel width, which agrees well with our experimental results which show that the device performance, such as mobility, subthreshold swing, and ON voltage, is improved with decreasing channel width.

Figure 9 shows the calculated threshold voltage as a function of channel width. The measured ON voltage shown in Fig. 3 is also re-plotted here for comparison. The channel width dependence on the calculated threshold voltage and ON voltage is indeed quite similar. Note that the calculated threshold voltage is slightly smaller than the ON voltage by...
Table 1. Summary of the fitting parameters used to simulate poly-Si TFTs with \( W/L = 10 \mu m/20 \mu m \) and \( 0.9 \mu m/20 \mu m \).

<table>
<thead>
<tr>
<th>( N_{td} ) (cm(^{-2}))</th>
<th>( E_{td} ) (eV)</th>
<th>( N_{tt} ) (cm(^{-2}))</th>
<th>( E_{tt} ) (eV)</th>
<th>( V_{th} ) (V)</th>
<th>( V_{fb} ) (V)</th>
<th>( \mu_0 ) (cm(^2)/V.s)</th>
<th>( \alpha )</th>
</tr>
</thead>
<tbody>
<tr>
<td>( W = 10 \mu m )</td>
<td>1.3 ( \times 10^{12} )</td>
<td>0.15</td>
<td>3.85 ( \times 10^{12} )</td>
<td>0.4</td>
<td>7.0</td>
<td>1.0</td>
<td>80</td>
</tr>
<tr>
<td>( W = 0.9 \mu m )</td>
<td>1.06 ( \times 10^{12} )</td>
<td>0.15</td>
<td>3.6 ( \times 10^{12} )</td>
<td>0.4</td>
<td>5.5</td>
<td>1.0</td>
<td>80</td>
</tr>
</tbody>
</table>

5. Conclusions

We have fabricated and systematically characterized poly-Si TFTs with various channel widths ranging from 10 \( \mu m \) to 0.9 \( \mu m \). We found that the TFT characteristics, such as mobility, threshold voltage, and subthreshold swing, are dramatically improved with reducing channel width, especially when the channel width is less than 2 \( \mu m \). A simple physically-based model is proposed to extract the amounts of deep state density and tail state density. By considering both the deep and tail states, excellent fitting with experimental data is achieved over a wide range of drain bias, gate bias, and channel width. Our results also show that both the deep state density and tail state density are reduced with channel width, thus accounting for the improved TFT characteristics with reducing channel width.

Acknowledgements

The authors would like to thank National Science Council in Taiwan for the financial support of this study (NSC91-2215-E-110-019).