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Short-Channel Poly-Si Thin-Film Transistors with Ultrathin Channel and Self-Aligned Tungsten-Clad Source/Drain

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A short-channel polycrystalline silicon (poly-Si) thin-film transistor (W/L = 10 μm/3 μm) with an ultrathin channel (30 nm) and self-aligned tungsten-clad source/drain structure is demonstrated. With WF₆ and SiH₄ gas flow ratio of 40/12, selectively deposited tungsten film over 100 nm thick can be easily grown on source/drain regions. As a result, the parasitic source/drain resistance is greatly reduced, leading to improvement of device driving ability. Because tungsten deposition can be carried out at a low processing temperature of 300°C, the proposed simple structure is compatible with conventional top-gate structure and can be readily applied to low-temperature poly-Si fabrication.

Recently, polycrystalline silicon (poly-Si) thin-film transistors (TFTs) have been attractive as applications in peripheral circuits for active matrix liquid-crystal displays (AMLCDs). To achieve higher speed and circuit densities, it is necessary to scale down device dimensions. However, short-channel poly-Si TFTs suffer from severe kink effect due to the presence of a floating body. Specifically, holes generated by impact ionization accumulate in the body and raise its potential, which turns on the parasitic bipolar junction transistor (BJT). Minimizing the body region by using a thin channel can alleviate the floating body effect effectively. However, thin source/drain (S/D) regions with large series resistance also degrade device performance. To reduce this series resistance, many methods have been proposed to fabricate a raised source/drain structure.

However, for ultrathin-channel poly-Si TFTs, reducing S/D resistance by self-aligned silicide (SALICIDE) or selective tungsten chemical vapor deposition (SWCVD) technologies have not been studied before. SWCVD is a good candidate to reduce S/D resistance because of its small Si consumption. In this paper, short-channel poly-Si TFTs with ultrathin channel and tungsten-clad S/D (W-TFTs) are proposed. With a simple process step and conventional top-gate structure, W-TFTs can suppress the floating body effect and obtain improved driving current simultaneously.

Experimental

First, a 30 nm amorphous silicon layer was deposited by low-pressure chemical vapor deposition (LPCVD) at 550°C on oxidized silicon wafers. After active region patterning, a 60 nm tetraethylorthosilicate (TEOS) oxide layer and subsequently a 300 nm amorphous silicon layer (a-Si) were deposited by LPCVD. The a-Si layer was then recrystallized by solid-phase crystallization (SPC) at 600°C for 24 h. After defining gate by reactive ion etching (RIE) and removing the oxide on S/D regions by HF dip, n⁺ lightly doped drain (LDD) implant was performed using phosphorus ions at a dose of 3 x 10¹⁵ cm⁻². Then, a 200 nm oxide sidewall spacer was formed abutting the gate by conformal deposition of a TEOS oxide layer and subsequent RIE. Next, phosphorus ions at a dose of 5 x 10¹⁵ cm⁻² were implanted to form the n⁺ S/D region. Doping was activated by rapid thermal anneal (RTA) at 750°C for 20 s. After removing the remaining oxide on S/D regions by diluted HF, wafers were loaded into a W-CVD system (ULVAC ERA-1000) to selectively deposit W film on the exposed gate, source, and drain regions. The selective deposition was first dominated by a silicon reduction reaction, which has a self-limiting nature to consume silicon less than 20 nm. After the formation of an initial thin W film, a SiH₄ reduction reaction took place with a deposition rate of approximately 240 nm/min. The WF₆/SiH₄ gas flow rate was kept at 40/12 and the process temperature was 300°C. Conventional devices without W film deposition were also fabricated to serve as controls. A 500 nm Al film was deposited, patterned, and sintered at 400°C for 30 min to form metal pads. To reduce trap density and improve interface quality, wafers were also immersed in an NH₃ plasma generated by plasma-enhanced CVD (PECVD) at 300°C for 1 h. For W-TFTs, wafers were split to receive the NH₃ plasma treatment either before or after W deposition to study the effects of W-clad S/D structure on blocking the NH₃ molecules from entering the active channel region. A cross-sectional scanning electron microscopy (SEM) image of the proposed W-TFT is shown in Fig. 1. A schematic structure is also drawn in the inset of Fig. 1. The W film is about 120 nm thick and the silicon consumption in S/D regions is limited to less than 20 nm. As a result, the contact resistance can be kept low, because the 30 nm channel film is not fully consumed.

Results and Discussion

Figure 2a depicts the output characteristics (I₅₋₁, V₉₋₁) of W-TFTs and their conventional counterparts without selective W deposition. The nominal channel width and length are 10 and 3 μm, respectively. W-TFTs exhibit a larger driving current than conventional poly-Si TFTs with ultrathin channel and tungsten-clad S/D (W-TFTs) are proposed. With a simple process step and conventional top-gate structure, W-TFTs can suppress the floating body effect and obtain improved driving current simultaneously. © 2003 The Electrochemical Society. [DOI: 10.1149/1.1635093] All rights reserved.
TFTs, especially under high gate bias. In a linear region, the TFT ON resistance, $R_{on}$, consists of channel resistance, $R_{ch}$, and the parasitic resistance, $R_{p}$. That is

$$R_{on} = \frac{\partial V_D}{\partial I_D} = R_{ch} + R_{p}$$  \[1\]

Because the channel resistance in the linear region is given approximately by

$$R_{ch} = \frac{L}{W\mu C_i (V_G - V_{TH})}$$  \[2\]

where $C_i$ is the gate dielectric capacitance per unit area and $W$, $L$, and $V_{TH}$ are device channel width, length, and threshold voltage, respectively. The parasitic resistance $R_{p}$ of W-TFTs can be extracted by plotting width-normalized $R_{on}$ vs. $L$ as in Fig. 2b. The width-normalized $R_{on}$ vs. $L$ curves merge at $L = 0.84 \mu$m and have a residual value of a gate-voltage independent $R_{p}$ of 4 kΩ. The $R_{p}$ of the conventional TFTs is also extracted by the same method and is 13.5 kΩ, which is three times larger than that of W-TFTs. In our experiment, the $R_{p}$ consists of the S/D resistance and the series resistance in LDD regions. With identical ion implantation conditions and activation annealing process, the difference in the LDD resistances may be ignored. As a result, the small $R_{p}$ of W-TFTs is mostly due to the decreased S/D resistance.

To examine the floating body effect of the ultrathin-channel W-TFTs, the threshold voltages ($V_{TH}$) roll-off of W-TFTs and conventional TFTs are compared in Fig. 3. The $V_{TH}$ is determined by the constant drain current method. The $V_{TH}$ of W-TFTs with thick channel region (~50 nm) is also plotted in Fig. 3 for comparison. Apparently, $V_{TH}$ roll-off of W-TFTs with thick channel is much more pronounced than that of ultrathin-channel W-TFTs, revealing that an ultrathin channel effectively suppresses the floating body effect. Moreover, the $V_{TH}$ roll-off of ultrathin-channel W-TFTs is less severe than that of conventional ones with consistent channel thickness.

Figure 2. (a) Output characteristics of W-TFTs and conventional TFTs with channel thickness = 30 nm, and dimension $W/L = 10 \mu$m/3 $\mu$m. (b) The width-normalized ON resistance of W-TFTs as a function of channel length. The channel width is fixed as 10 $\mu$m while the channel length is varied from 10 to 3 $\mu$m.

Figure 3. Threshold voltage $V_{TH}$ of W-TFTs and conventional TFTs with channel length varying from 10 to 0.8 $\mu$m, the channel width is kept as 10 $\mu$m and the channel thickness is 30 nm. $V_{TH}$ of W-TFTs with 50 nm channel film is also plotted to make a comparison.

Figure 4. Transfer characteristics of W-TFTs with (a) plasma treatment before W deposition and (b) plasma treatment after W deposition.
thickness. A plausible reason is that the metal-silicon interface increases hole injection from body to source, leading to the suppression of the floating body effect.\(^8\)

Additionally, we discuss the efficiency of NH\(_3\) plasma passivation when fabricating W-TFTs. The transfer characteristics (\(I_D - V_G\)) of W-TFTs with plasma passivation performed either before or after tungsten deposition are compared in Fig. 4. Apparently the latter ones depict higher threshold voltage and degraded subthreshold swing. This is because the W film deposited around a S/D region and polysilicon gate effectively blocks NH\(_3\) molecules from entering the active channel region. Fortunately, plasma hydrogenation can be performed before W deposition, with passivated dangling bonds remaining stable during W deposition at 300°C, the same temperature as the NH\(_3\) plasma treatment. Finally, the threshold voltage and subthreshold swing (\(S.S.\)) of W-TFTs that receive passivation before W deposition are extracted to be 0.68 V and 0.29 V/dec, which are comparable to those of their conventional counterparts (\(V_{TH} = 0.62\) V and \(S.S. = 0.3\) V/dec). This ensures good interface quality and junction integrity of the proposed W-TFTs.

**Conclusions**

We have proposed short-channel poly-Si TFTs with ultrathin channel and W-clad S/D structure. The experimental results show that the new devices depict improved turn-on characteristics by successfully reducing the S/D resistance. Less pronounced threshold voltage roll-off is also observed, which may be explained by enhanced hole injection from body to source for W-TFTs. Plasma passivation before tungsten deposition is also important for obtaining good passivation efficiency.

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