Reliability studies of Hf-doped and NH₃-nitrided gate dielectric for advanced CMOS application


Abstract: A novel technique is proposed for forming high-K dielectric of HiSiON by sequentially doping base oxide with Hf and nitridation with NH₃. The HiSiON gate dielectric demonstrates excellent device performances such as only 10% degradation of saturation drain current and almost 45 times of magnitude reduction in gate leakage compared to conventional SiO₂ gate dielectric at the same equivalent oxide thickness (EOT). Additionally, negligible flatband voltage shift is achieved with this technique. Excellent performances in electrical stressing are also demonstrated by the dielectric.

1 Introduction

Recently, high-K gate dielectric films have been widely studied to replace SiO₂ for low power and small leakage current CMOS technology applications [1–3]. Among the reported high-K dielectrics, HfO₂ has attracted much attention as a promising candidate due to high dielectric constant, wide band-gap, and compatibility with poly–Si [4]. However, some techniques have been proposed [1–3, 5] to improve the properties of high-K film, some critical issues such as obvious mobility degradation and large flatband voltage shift still existed, thus impeding its real applications for device and circuit.

The mobility degradation is due to the surface states or defects at the HfO₂/Si interface and the large positive flatband voltage shift to the existed negative charges in HfO₂ dielectric. Hence, in this study, we developed a novel method for preparation of high-K dielectric to solve those issues. First, the base oxide was thermally grown and then doped with hafnium (Hf). Next, the doped oxide was nitrided with nitrogen (N₂) to form HiSiON high-K dielectric. With the method, the interface states or defects could be reduced or eliminated by the thermally grown base oxide, and the negative charges indielectric could be compensated with the positive charges induced by the incorporated nitrogen, thus improving the mobility degradation and flatband voltage shift. In comparison to the reported techniques, the proposal possesses the advantages of less degradation of mobility, higher drain current and the negligible flatband voltage shift.

2 Experimental

N+ NMOSFETs with polycrystalline-silicon gates were fabricated on p-type (100) silicon wafers using 0.1μm CMOS technology. After a standard SCI/SC2 wet clean, 1.7nm base oxides were thermally grown in O₂ ambient. Then, the base oxides were doped with Hf (hafnium) using HCl₄ at substrate temperature of 300°C by atomic layer chemical vapour deposition (ALCVD), and sequentially annealed in NH₃ under 950°C for 60 seconds to form the HiSiON. Conventionally ALCVD deposited HfO₂ (ALD_HfO₂) films were also prepared by using HCl₄ and H₂O in cycles. Next, a 150 nm thick undoped poly–Si film was deposited and patterned, followed by phosphorus of 25 keV implantation with dose of 1 × 10¹⁵ cm⁻² to form the N+ poly–Si gate. Then spike activation was carried out at 1050°C. In comparison, control oxides were prepared by wet oxidation of the Si substrate directly. Finally, interlayer deposition (ILD), W-plug formation and Cu interconnection were conducted sequentially, followed by forming gas annealing at 400°C for 30 min. Additionally, for the measurement of flatband voltage shift and extraction of equivalent oxide thickness (EOT), capacitors with split dielectrics were also prepared with the same process for NMOSFET samples, except for the larger area of 1000μm square and the S/D being connected together.

Current–voltage (I–V) and capacitance–voltage (C–V) characteristics were obtained from HP 4156B precision semiconductor parameter analyser and HP 4284A precision LCR meter measurements, respectively. On the other hand, a C–V simulator, which took into account both poly–Si depletion and quantum mechanical effects [6], was used to extract EOT and V_{FB} values.

3 Results and discussions

Figure 1 shows the SIMS analysis of the HiSiON sample. The existence of HiSiON layer is identified by the presence of nitrogen, oxygen, and hafnium (Hf). In the Figure, the scale of hafnium (Hf) signal on the right vertical axis was enlarged for the lower sputtering yield of hafnium with heavy atomic mass. Based on the C–V measurement, for various gate dielectrics, i.e. SiO₂, HiSiON, and ALD_HfO₂, the extracted EOT and V_{FB} for SiO₂, HiSiON and
HfO₂ dielectrics are 15.7 Å, –1.09 V; 16 Å, –1.08 V and 18 Å, –0.8 V, respectively. Obviously, the flatband voltage of HfO₂ is shifted positively against the SiO₂ and implies the existing of negative charges in HfO₂ [1, 2, 5]. On the other hand, negligible flatband voltage shift against SiO₂ is found in the HfSiON sample. In the past, we found [7] the doped nitrogen will generate positive charges in gate dielectric. Therefore, we attribute the negligible flatband voltage shift in HfSiON to the compensation of negative charges with the positive charges generated by the nitrogen incorporated in HfSiON. The leakage currents measured at 1 V are about 78 mA/cm², 0.1 mA/cm² and 3.24 A/cm² for HfSiON, HfO₂ and SiO₂ dielectrics, respectively. The leakage current through HfSiON dielectric is almost 45 times the reduction in magnitude to the SiO₂ gate dielectric at same EOT. Because of the physical thickness of HfO₂, HfSiON, and SiO₂, measured from TEM and shown in the Fig. 2, are 39.2 Å, 24 Å, and 17.6 Å, respectively, it is reasonable to attribute the reduction in leakage of HfSiON and HfO₂ to their thicker physical thickness. Based on the measured thickness, the extracted k-value is about 5.85 for HfSiON dielectric. Although this value is lower than 10, it could be raised by doping more hafnium into the base oxide and optimising the nitridation process. Since, the preparation of HfSiON is doped with hafnium (Hf) and then nitrided with NH₃ on a base oxide (SiO₂). The content of Hf and nitrogen in SiO₂ should affect the dielectric’s permittivity.

Although even the HfO₂ possesses the least leakage current, it also suffers a large number of defects or surface states in the HfO₂/Si channel interface, thus degrading the drain current for future CMOS technology applications. The \( I_{ds} - V_{gs} \) curves are shown in Fig. 3. It is clear that threshold voltage for HfO₂ is too large for 0.1 μm device application at this stage. Using our method, well-behaved \( I_{ds} - V_{gs} \) curve can be achieved. Figure 4 presents the drain current versus drain voltage (\( I_{ds} - V_{ds} \)) curves of short channel NMOSFETs with \( W/L = 10/0.1 \) μm under various normalised gate biases (\( V_{gs} - V_{th} \)). The gate voltage has been normalised with respect to threshold voltage to minimise the effect of threshold voltage. The measured drain currents at \( V_{gs} - V_{th} = 1 \) V are about 9.5 mA, 10.5 mA, and 2.6 mA for HfSiON, SiO₂ and HfO₂, respectively. Almost three-fourths degradation in magnitude of Idsat for HfO₂ with respect to SiO₂, but only 10% degradation for HfSiON to SiO₂ is found. Based on the C–V curves and \( I_{ds} - V_{gs} \) curves, the extracted mobility values at effective field of 1 MV/cm are 267, 216, and 103 cm²/V·s for SiO₂, HfSiON, and HfO₂, respectively. The Idsat for NMOSFET with high-K gate dielectric. We assume the thermally grown 1.7 nm base oxide in the proposed HfSiON
gate dielectric releases the stress at the interface of HfSiON/Si, thus eliminating the interface states or defects and resulting in the large \( I_{dsat} \). Excellent device performances are obtained using this technique. Next, the trapping and reliability characteristics of the HfSiON gate dielectric are executed and compared to SiO\(_2\). Figure 6 shows the C–V measurements (at 100 kHz) of NMOS capacitors with HfSiON dielectric before and after stressing at 1.6 V under 140°C for 1 hour. The flatband voltage shift is less than 10 mV, indicating good stability under stress. Figure 7 demonstrates the charge-trapping characteristics of NMOS capacitors with HfSiON and SiO\(_2\) dielectrics at both gate polarities. Less trap generation for HfSiON is observed. Figure 8 displays the stress-induced leakage current (SILC) of NMOS capacitors measured at -1 V under constant voltage stressing (CVS) of -3 V. The SILC of the MOS capacitor with SiO\(_2\) increases significantly after 100 s stressing, but the SILC of the MOS capacitor with HfSiON increases only after 800 s stressing.

4 Conclusion

The experimental results in this study indicate that a base oxide doped with hafnium (Hf) and sequentially nitrided with NH\(_3\) forms the HfSiON high-K dielectric can effectively suppress flatband voltage shift, and significantly

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**Fig. 4** Drain current against drain voltage \((I_d-V_{ds})\) curves of the short channel NMOSFETs with \(W/L=100/0.1\) \(\mu\)m under various normalised gate biases

Measured drain current at \(V_{gs}-V_{th} = V_{ds} = 1\) V are 9.5 mA, 10.5 mA and 2.6 mA for HiSiON, SiO\(_2\) and HfO\(_2\), respectively

**Fig. 5** Extracted mobility values for SiO\(_2\), HfSiON, and HfO\(_2\) based on C–V and \(I_d-V_{ds}\) measurements

Respective values are 216 and 103 cm\(^2\)/V-s at effective field of 1 MV/cm

**Fig. 6** C–V curves of HiSiON gate dielectric before/after stressing at 1.6 V under 140°C for 1 h

Frequency of C–V measurement is 100 kHz
improve drain saturation current. The improvements in the HfSiON high-K dielectric are attributed to the charges compensation induced by the incorporation of nitrogen and the elimination of surface states or defects in the gate dielectric/channel interface with the thermally grown base oxide. In addition, excellent performances in electrical stressing demonstrate good film qualities.

5 Acknowledgments

The authors would like to thank the members of R&D in Taiwan Semiconductor Manufacturing Co., Ltd., for wafer fabrication and technical supports. The work was financially supported by the National Science Council under Contract NSC92-2215-E-006-016.

6 References