Crossbar array of selector-less TaOx/TiO2 bilayer RRAM

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ABSTRACT

In this work, we have implemented self-rectifying TaOx/TiO2 RRAM in a selector-less 6 × 6 crossbar array with various desiring features, including: (1) simple fabrication using only three masks, (2) high self-rectifying ratio up to 10^3 for sneak current suppression, (3) stable bipolar resistive-switching characteristics without the need for electro-forming and current compliance, (4) data retention time over 10^4 s, and (5) robust READ and WRITE disturb immunity. Finally, an achievable array size of 1 Mb was simulated using an All-LPU read scheme and a V/3 write scheme.

1. Introduction

Resistive Random Access Memory (RRAM) is one of the most promising emerging memory technologies because of its non-volatility, high write speed, and simple structure which offers excellent scalability and high bit density with its 4F2 cell size. However, when integrating RRAM cells into a passive crossbar memory array, the sneak current issue limits the maximum array size [3]. Thus, an additional selection device connected to every cell is required to suppress the sneak current. Most common configurations for crossbar array cells are one bipolar selector—one resistor (1S1R) [3–6] and one diode—one resistor (1D1R) [7], depending on the type of selection device used. While maintaining the compact cell footprint of 4F2 is possible by vertically stacking the selection device with RRAM [3,6], such approaches will inevitably increase the complexity of the fabrication process. The detailed device requirements, integration and material considerations as well as state-of-the-art in the field of crossbar memory arrays and selection devices are thoroughly summarized in several recent review papers [8,9]. It has to be noted, that the requirements for the selection devices are indeed highly challenging. Not only should the selection device support ON-state current density in the order of several MA/cm2 while maintaining OFF-state leakage current as low as possible, its performance should exceed all specifications for RRAM including response time, cycling endurance, array yield, and variability, in order not to limit the overall memory chip performance and reliability [9].

Therefore, one of the most promising solutions in minimizing the cell area footprint and fabrication complexity is the RRAM cell with highly non-linear I–V characteristics (also called selector-less or self-rectifying), which does not require an additional selection device. Such a cell design typically employs a bi-layered dielectric, like TiO2/HfO2-based RRAM with Ni electrodes shown in our previous work [10], or TaOx/HfOx [11], HfO2/TaOx [12], HfO2/TiON [13] and TiO2/Al2O3 [14] based RRAM cells recently demonstrated by other groups. We have recently fabricated a self-rectifying Ta/TaOx/TiO2/Ti RRAM cell featuring forming free and self-compliant operation for simplifying peripheral circuit design, high self-rectification ratio for high-density memory array, ultra-high endurance over 10^12 cycles, and multi-level-cell (MLC) capability [15,16]. As opposed to a filamentary switching (formation and rupture of conductive filaments) mechanism commonly responsible for resistive switching in most of the single layer (and also some multi-layer) oxide devices [17], the switching in this TaOx/TiO2-based bilayer device was ascribed to oxygen ion migration driven by bipolar electric field, and the corresponding modulation of the Schottky barrier tunnel width at the Ta/TaOx interface. More details about the properties of this RRAM cell and detailed discussion on the switching mechanism has been given elsewhere [16]. However, most of these studies on selector-less RRAM focus on the single-cell characteristics, experimental demonstrations of selector-less (1R) crossbar arrays based on binary oxide dielectrics have yet to be investigated. Such demonstrations allow array-level evaluations on the interference and disturb properties at READ and WRITE, all critical for implementing high-density crossbar arrays.

In this study, the self-rectifying TaOx/TiO2 bilayer RRAM was successfully implemented into a proof-of-concept 6 × 6 passive selector-
less crossbar array by using only three masks while maintaining the main features of the standalone RRAM cell. Robust READ and WRITE interference and disturb immunity in the array was experimentally demonstrated. Moreover, the simulation results have shown a feasibility of 1 Mb array size using an All-Line-Pull-Up (All-LPU) read scheme [18, 19] and a V/3 write scheme [20].

2. Material and methods

Three different shadow masks were used to pattern the 6 × 6 crossbar RRAM array, as shown in Fig. 1. First, 100-nm thick Ti word-line electrodes were deposited using dc magnetron sputtering with a Ti (99.99%) target at a deposition rate of 1 nm/s. The first shadow mask with a 200-μm line-width was used to define the electrode patterns. To prepare the TaOx/TiO2 resistive switching bilayer, 60-nm thick TiO2 and 20-nm thick TaOx were sequentially deposited through the second shadow mask by means of reactive dc magnetron sputtering using Ti (99.99%) and Ta (99.95%) targets, respectively, in an Ar/O2 gas mixture. Finally, 100-nm thick and 200-μm wide Ta bit-line electrodes, running perpendicularly to the word-line electrodes (Fig. 1), were defined using the third shadow mask and deposited by dc magnetron sputtering with a Ta (99.95%) target at a deposition rate of 0.1 nm/s. The top-view optical microscope image of the unit cell is shown in the inset of Fig. 2, where the violet dog-bone shape region is the resistive-switching oxide bilayer sandwiched between horizontal word lines and vertical bit lines. During the measurement procedure, the voltage bias was always applied to the Ta bit-line electrodes and the Ti word-line electrodes were grounded.

3. Results and discussion

Fig. 2 shows typical bipolar resistive-switching (BRS) characteristics for a single RRAM cell. This device requires neither electrical forming nor current compliance for its operation, significantly reducing the complexity of the peripheral circuit design. The cell is switched to the Low Resistance State (LRS) with no obvious SET transition by sweeping the voltage in the positive polarity up to +6.0 V. The TiO2/Ti interface is believed to be an ohmic contact [21], so the current at a positive bias is limited mainly by the conduction band offset at the TaOx/TiO2 interface which is not influenced by the SET process. However, the charge distribution near the Ta/TaOx interface is affected by O2− migration during SET and this results in the reduced tunnel width of the Ta/TaOx Schottky barrier [16]. Therefore, the device shows a clear memory window in the negative polarity. By performing a negative voltage sweep up to −4.0 V, the cell can be switched to its High Resistance State (HRS) by a gradual
RESET transition and this can be clearly observed particularly during the first negative voltage sweep (blue circles in Fig. 2). After several subsequent I–V loops (dashed lines in Fig. 2) the LRS current becomes lower and stabilizes in the order of ∼μA at a reading voltage $V_{\text{Read}} = -2.0 \text{ V}$. More details about the switching mechanism, including the schematic diagrams, band diagrams and simulated I–V curves, has been recently published elsewhere [16].

The stable memory window (HRS/LRS resistance ratio) at $V_{\text{Read}} = -2.0 \text{ V}$ is higher than 10×, as indicated in Fig. 2. Moreover, when compared to a positive-bias current at +2.0 V, this device shows a rectifying ratio (RR) at ±2.0 V of three orders of magnitude. This self-rectifying character is one of the major advantages of this cell design, effectively suppressing sneak-path currents during read operation when implemented in a selector-less 1R crossbar array.

![Fig. 5. Stable BRS operation of the selected cell which was initially in HRS while the neighboring unselected cells were in LRS (worst case scenario).](image)

Fig. 5 displays the typical current cumulative distribution read at −2.0 V in both HRS and LRS vs. the current at +2.0 V acquired during 100 BRS cycles on a single cell. The retention measurement results of both resistance states are displayed in Fig. 4. Both memory states display excellent stability and the memory window of about 10× was maintained for the entire duration of the measurement (16,200 s).

If a passive crossbar array is composed of cells with a rather linear (non-self-rectifying) I–V characteristics without additional selection devices (1R array), addressing a cell in a HRS might fail and result in a false reading of LRS. This might happen due to a current flowing through other neighboring LRS cells in the array, forming a sneak current path. The worst case scenario for misreading the selected HRS cell is when all unselected cells are in LRS. In order to evaluate the operation of our selector-less passive crossbar array employing self-rectifying Ta/TaO$_x$/TiO$_2$/Ti cells, we have performed BRS cycling of a selected cell in a 2 × 2 sub-array under the worst case scenario, with all three neighboring unselected cells in LRS. Their corresponding LRS currents read at $V_{\text{Read}} = -2.0 \text{ V}$ were 2.14 μA, 2.18 μA and 0.69 μA. As shown in Fig. 5, programming and reading both LRS and HRS of the selected cell were successful and reproducible, while the HRS currents were in the order of $10^{-7} \text{ A}$. This result demonstrates that the READ and WRITE operations in this 1R array are not interfered by the unselected cells.

Also, one or more writes (SET operations) performed on the selected cell might lead to a WRITE disturb of the neighboring unselected cell, i.e., the unintentional change of its resistance state. Similarly, a reading of the resistance state of the selected cell might lead to a READ disturb of the neighboring unselected cell. Fig. 6 displays the cycling measurement of a two neighboring cells under a READ scenario where the cell(1,1) is cycled between LRS and HRS while the resistance state of the neighboring cell(1,2) is switched every five cycles. Both cells are read in each cycle, showing excellent READ and WRITE disturb immunities.

The yield of the working cells in this 6 × 6 array was around 70%, as shown in Fig. 7. Switchable (working) cells in this array were operated at least for five consecutive BRS cycles with satisfactory memory windows. Because the dimension of our proof-of-concept 6 × 6 array was rather large (3 × 4.5 cm$^2$) by using the shadow-mask process, most failed devices were located at the array edge, which might be attributed to the unoptimized uniformity of the film deposition. It has to be noted, that although all the failed (non-working) cells were showing no or little memory window, they kept their self-rectifying character, and thus did not interfere with the correct readout of memory states in other working cells, as opposed to single layer RRAM cells which tend to be highly conductive (short) when defective. The self-rectifying character is attributed to the bilayer resistive-switching oxide structure used in our cells [16].

Finally, we have performed a HSPICE-based simulation to estimate the maximum attainable array size [18,19], taking into account the self-rectifying characteristics of our RRAM cells. Using an All-Line-Pull-Up (All-LPU) read scheme with a reading voltage of −2.55 V, a V/3 write scheme [20], and an interconnect line resistance ($R_c$) of 2.5 Ω/□,
an array size of 1 Mb is feasible using a criterion of 10% read margin (Fig. 8a) and 75% write access voltage (Fig. 8b). The reading voltage higher than −2.0 V (used throughout this work) was chosen because of the additional voltage drop on the pull-up resistor and interconnect lines. The actual voltage sensed by the cells would be closer to −2.0 V. Concerning write operations, the resistances of interconnect lines have more significant influence on the attainable array size during RESET operation (Fig. 8b), as the resistance at the selected cell is lower during RESET than during SET (Fig. 2).

4. Conclusions

In this paper, a self-rectifying Ta/TaO x/TiO 2/Ti bilayer RRAM was successfully implemented into a 6 × 6 passive selector-less 1R crossbar array by using a simple three-mask process. The sneak current issue causing READ and WRITE interference was suppressed owing to a sufficient self-rectifying ratio. In addition, robust READ and WRITE disturb immunity was also experimentally demonstrated. Finally, the simulation results indicated that the maximum attainable size of the proposed selector-less crossbar array can be up to 1 Mb, showing the promise for future high-density memory applications.

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References