Homework 7: MOSC & MOSFET Theory
(Due on 6/7 in Class)

1. (High-k dielectrics in MOSC) We will consider putting different insulators in the gate dielectric now. This is an important direction in logic and memory CMOS technology. We will practice two of the most popular ones, although the eligible dielectrics have been thoroughly investigated according to the periodic table by the industry. The silicon nitride, with a nominal Si₃N₄ composition (but not a constant composition), has a typical energy band distribution of (2.0eV, 2.0eV, 1.1eV, 3.0eV) in (affinity, $\Delta E_C$ with silicon, silicon band gap, and $\Delta E_V$ with silicon) and a relative dielectric constant of 9.0. Hafnium oxide, with a composition of HfO₂, has an energy band distribution of (2.5eV, 1.5eV, 1.1eV, 2.5eV) and a relative dielectric constant of 20. Both nitride and HfO₂ form a type-I heterojunction with silicon and SiO₂. We will have a p-type substrate with $10^{17}$cm⁻³ homogeneous $N_A$ doping. We will use a metal work function that gives flat band at $V_G=0$.

(a) For a gate stack of SiO₂/Si₃N₄/SiO₂ (6nm/6nm/2nm) to replace the original SiO₂ (this is called the MONOS or SONOS device), draw the band diagram at flat band and at the onset of inversion. Calculate the electric fields and potential drops in the three layers of SiO₂/Si₃N₄/SiO₂ at onset of inversion. (16 pts)

(b) What is the surface potential at strong inversion? What is the threshold voltage $V_{th}$? What is the effective oxide thickness (EOT) that will give the same $V_{th}$ but the entire stack is SiO₂? (10 pts)

(c) Repeat (a) and (b) with a gate stack of HfO₂/SiO₂ (3nm/0.5nm). This is the composition of the Hafnium announcements by Intel and IBM in January 2007. (20 pts)

2. (Gate current reduction in high-k dielectric) For the gate stack for logic devices of Prob. 1(c), i.e., the gate stack of HfO₂/SiO₂ (3nm/0.5nm).

(a) In comparison with the pure SiO₂ gate dielectric with the same EOT, assuming $V_G=1$V and the gate work function of 5.1eV and substrate doping of $N_A=10^{17}$cm⁻³, calculate the electric field in SiO₂ in pure SiO₂ gate dielectric, and in SiO₂ and HfO₂ in the high-k gate stack. (6 pts)

(b) Can F-N tunneling happen at either of the gate stack at $V_G=1$V? Briefly explain. What will be the dominant mechanism of gate current for both gate stacks at $V_G=1$V? (6 pts)

(c) At what $V_G$ (both negative and positive) will F-N tunneling start for both gate stacks? (6 pts)

(d) Do you expect the $I_G-V_G$ curve to be symmetrical (i.e., the magnitude of $I_G$ the same for the same magnitude of $V_G$)? Briefly explain. (6 pts)

(e) If SiO₂ has a breakdown field of $1.5\times10^7$V/cm and HfO₂ of $6\times10^6$V/cm, what is the highest positive $V_G$ that the two gate stacks can sustain? In the HfO₂/SiO₂ gate stack case, which layer will break down first? (6 pts)

3. (Subthreshold operations) For a long-channel nMOSFET with $t_{ox}=2.4$nm and $N_{sub}=2\times10^{17}$cm⁻³,

(a) Estimate the subthreshold slope $S$ in mV/decade not very far away from strong inversion. (6 pts)

(b) To obtain $I_{ON}/I_{OFF}=10^7$, what is the minimal voltage swing? (6 pts)

(c) If $S$ needs to be less than 90mV/decade under the constraint of fixed $t_{ox}=2.4$nm, what is the constraint on $N_{sub}$? (6 pts)

(d) For the gate stack of HfO₂/SiO₂ (3nm/0.5nm) with the same $N_{sub}=2\times10^{17}$cm⁻³, what is your estimate of $S$ now? (6 pts)